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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,034	12/04/2001	Nobuharu Kobayashi	ASAM.0032	9304

EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2187	

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DATE MAILED: 10/28/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/000,034	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	NGOC V DINH	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 04 December 2001 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-11,13 and 16 is/are rejected.

7)☒ Claim(s) 12, 14-15, 17-18 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

PRIORITY DOCUMENT

1. The application filed on 12/04/01 indicated that the serial number of the certified copy of the priority document is 2000-367874.

However, a further review showed that there is an additional priority document (2001-15110) also submitted along with the priority document mentioned above. Accordingly, the priority document 2001-15110 appears to belong to other Applicant's application.

INFORMATION DISCLOSURE STATEMENT

2. The Applicant's submission of the IDS filed 12/04/01 have been considered. As required by M.P.E.P. 609 C(2), a copy of the PTOL-1449 is attached to the instant office action.

Claim Objections

3. Claim objected to because of the following informalities:

Claim 6, line 7, "signa" should be replaced with – signal --.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6-11, 13 and 16 are rejected under 35 U.S.C.102 (e) as being anticipated by Miyamoto et al PN 6,429,719.

4. As per claims 1, 6:

Miyamoto teaches a semiconductor device [fig. 1, 2-4, 7] comprising: a first input/output interface circuit [SCI, fig. 7] adapted to a serial bus; an internal circuit [DMAC, fig. 7] for performing a circuit operation corresponding to a signal which is inputted or outputted through said first input/output interface circuit between said

internal circuit and said serial bus; a non-volatile storage circuit [Flash, fig. 7] for storing identification data [e.g., security management information, col. 15-55]; a comparator circuit [CMT, fig. 7; col. 12, lines 1-20] for comparing internal identification data stored in said non-volatile storage circuit with external identification data included in an input signal supplied through said serial bus; and a control circuit [DTC, fig. 7; col. 10, lines 1-35] responsive to an input signal subsequently supplied through said serial bus when said comparator circuit generates a match detecting signal for performing a circuit operation corresponding to said input signal; circuit operation performed by said control circuit includes: an operation for re-writing identification data into said non-volatile storage circuit in response to said input signal; and an operation directed to said internal circuit in response to said input signal [fig. 7-8; col. 9, lines 13-65; col. 11, line 53 to col. 12, line 30; col. 37, lines 5-65].

5. As per claim 7:

Miyamoto teaches a semiconductor device further comprising: wiring means adapted to said serial bus, said wiring means having one end connected to said first interface circuit; a second input/output interface circuit connected to the other end of said wiring means; and a signal processing circuit provided through said second input/output interface circuit, wherein: said second input/output interface circuit and said signal processing circuit are mounted in a first semiconductor chip, and said first input/output interface circuit, said internal circuit, said non volatile storage circuit, said comparator circuit and said control circuit are mounted in a second semiconductor chip, and said first semiconductor chip and said second semiconductor chip are integrally encapsulated into said semiconductor device [fig. 2-4; col. 7, line 55 to col. 8, line 67; col. 9, lines 1-50].

6. As per claim 8-11:

Miyamoto teaches a semiconductor device, wherein: said wiring means comprises: first bonding wires for connecting bonding pads corresponding to said second input/output interface circuit in said first semiconductor chip to associated leads; and

second bonding wires for connecting bonding pads corresponding to said first input/output interface circuit in said second semiconductor chip to associated leads; wherein: said signal processing circuit in said first semiconductor chip includes a processor unit, and a ROM for storing a signal processing procedure performed by said processor unit, and said internal circuit in said second semiconductor chip includes a memory circuit which is allocated an address space difference from an address space allocated to said non-volatile storage circuit for storing said identification data; wherein: said memory circuit is comprised of memory cells each having the same structure as said nonvolatile storage circuit for storing said identification data [fig. 25-28; col. 2 to col. 4; col. 22 to col. 36].

7. As per claims 13, 16:

Miyamoto teaches a data processing system [fig. 1] comprising a plurality of semiconductor devices, each semiconductor device comprising: an input/output interface circuit adapted to a serial bus; an internal circuit for performing a circuit operation corresponding to a signal inputted or outputted through said input/output interface circuit between said internal circuit and said serial bus; and a non-volatile storage circuit for storing identification data, wherein the circuit operation performed by said internal circuit includes an operation for changing said identification data [e.g., read modify write]by an input signal supplied [e.g., RAS at low level/high level] through said serial bus when an internal state transitions to a first state [fig. 7; fig. 7-8; col. 9, lines 13-65; col. 11, line 53 to col. 12, line 30; col. 37, lines 5-65; col. 17, line 20-67; col. 18, lines 1-60].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4-5 is rejected under 35 U.S.C 103(a) as being unpatentable Miyamoto.

8. As per claims 2, 4-5:

Miyamoto teaches the claimed limitations as noted above.

Miyamoto does not explicitly teach internal identification data is read from said non-volatile storage circuit and transferred to a predetermined storage circuit under the condition that identification data stored in said non-volatile storage circuit transitions to a predetermined state; said predetermined state is set by a predetermined input signal which is first supplied through said serial bus after said semiconductor device is powered on; a reset signal input terminal, wherein: said predetermined state is set when a predetermined signal is inputted to said reset signal input terminal. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made because when manufacturing semiconductor device, various needs exist for testing the devices being fabricated in order to establish component grading. When testes are performed on semiconductor device, it is often necessary or preferable to hold identification data/code [input/output signal] at predetermined logic states to prevent unintended writing of data into memory, and further to avoid conflicts with other semiconductor device, which may be simultaneously under test. In any computer system, the reset signal is generally asserted in response to power being initially applied to the system or a computer system user pushing a "reset" button usually located on the computer system chassis. In response to the assertion of the reset signal, the semiconductor device enters a predetermined state, and then begins to provide data/instructions in response to CPU commands.

Claim 3 is rejected under 35 U.S.C 103(a) as being unpatentable Miyamoto, and further in view of Lin PN 6,184,724.

9. As per claim 3:

Miyamoto teaches the claimed limitations as noted above.

Miyamoto does not explicitly teach a supply voltage detector circuit for receiving a power supply voltage, wherein: said predetermined state is set when said supply voltage detector circuit detects that said power supply voltage rises to a first level. Lin teaches a supply voltage detector circuit for receiving a power supply voltage, wherein: said predetermined state is set when said supply voltage detector circuit detects that said power supply voltage rises to a first level [abstract; col. 3, lines 10-25; col. 9, lines 1-45].

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include voltage detector into Miyamoto semiconductor device. Doing so would allow the system to accurately, quickly and reliably determine the level of a semiconductor device supply voltage such that the semiconductor device can be optimally designed [col. 2, lines 1-60].

Allowable Subject Matter

10. As per claims 12, 14-15, 17-18:

Claims 12, 14-15, 17-18 are objected to as being dependent upon a rejected base claims 1, 13, 16 but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Landgraf PN 5,345,424 discloses power-up reset circuit for Flash memory.

b. Holtey et al PN 5,293,424 discloses Flash security memory card.

c. Oikawa PN 6,255,729 discloses Multichip package.

d. Davis et al PN 6,401,208 discloses method for BIOS authentication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (703) 305-3023. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks, can be reached on (703) 308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

NGOC DINH
Patent Examiner
Art Unit 2187
October 16, 2003

DONALD SPARKS
Supervisory Patent Examiner
Technology Center 2100